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# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet	1	of	2
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**Complete if Known**

<b>Application Number</b>	Not Yet Assigned
<b>Filing Date</b>	
<b>First Named Inventor</b>	Leonard Forbes
<b>Group Art Unit</b>	N/A
<b>Examiner Name</b>	Not Yet Assigned
<b>Attorney Docket Number</b>	M4065.0381/P381

U.S. PRO  
09/808114  
03/15/01

## U.S. PATENT DOCUMENTS

[illegible]

## FOREIGN PATENT DOCUMENTS

[illegible]

Examiner Signature	Kevin Quinto	Date Considered	11/27/02
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\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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PTO/SB/08B (08-00)  
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Substitute for form 1449A/PTO  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  <i>(use as many sheets as necessary)</i>				<b>Complete if Known</b>	
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Sheet	2	of	2	Attorney Docket Number	M4065.0381/P381

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS				
Examiner Initials	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issue number(s), publisher, city and/or country where published.		T <sup>2</sup>
72	A ✓	S. Tiwari, et al., "Straddle Gate Transistors: High I <sub>on</sub> /I <sub>off</sub> Transistors at Short Gate Lengths" IBM Research Division.		
	B ✓	W. Long, et al., "Dual-Material Gate (DMG) Field Effect Transistor."		
	C ✓	N. R. Rueger, et al. "Selective Etching of SiO <sub>2</sub> Over Polycrystalline Silicon Using CHF <sub>3</sub> in an Inductively Coupled Plasma Reactor."		
	D ✓	S. Vallon, et al., "Polysilicon-germanium Gate Patterning Studies in a High Density Plasma Helicon Source", J. Vac. Sci. Technol. A 15(4), Jul/Aug 1997.		
	E ✓	P. Patel, et al., "Low Temperature VUV Enhanced Growth of Thin Silicon Dioxide Films" Applied Surface Science 46 (1990) 352-356.		
	F ✓	W. Shindo, et al., "Low-Temperature Large-Grain Poly-Si Direct Deposition by Microwave Plasma Enhanced Chemical Vapor Deposition Using SiH <sub>4</sub> /Xe", J. Vac. Sci. Technol. A 17(5), Sep/Oct 1999.		
	G ✓	R. Nozawa, et al., "Low Temperature Polycrystalline Silicon Film Formation With and Without Charged Species in an Electron Cyclotron Resonance SiH <sub>4</sub> /H <sub>2</sub> Plasma-Enhanced Chemical Vapor Deposition", J. Vac. Sci. Technol. A 17(5), Sep/Oct 1999.		
	H ✓	C. Saha, et al., "Ion Assisted Growth and Characterization of Polycrystalline Silicon and Silicon-Germanium Films" (visited Nov. 18, 1999) <http://www.dialogselect.com/tech/cgi/pres>.		
	I	D. Landheer, et al., "Formation of High-Quality Silicon Dioxide Films by Electron Cyclotron Resonance Plasma Oxidation and Plasma-Enhanced Chemical Vapour Deposition" (visited Oct. 21, 1999) <http://www.dialogselect.com/tech/cgi/pres>.		
	J	K. Usami, et al., "Thin Si Oxide Films for MIS Tunnel Emitter by Hollow Cathode Enhanced Plasma Oxidation" (visited Oct. 21, 1999) <http://www.dialogselect.com/tech/cgi/pres>.		
	K	K.C. Saraswat, et al. "A Low Temperature Polycrystalline SiGe CMOS TFT Technology for Large Area AMLCD Drivers" (visited 11/18/99) <http://www.dialogselect.com/tech/cgi/pres>.		

Examiner Signature	Ken Quibb	Date Considered	11/27/02
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